3.3V GPS Receiver MMIC Implemented on a Mixed-Signal, Silicon Bipolar Array

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ABSTRACT

This generic GPS MMIC contains two downconversion stages and the dividers, buffers, digital phase-frequency detector and negative resistance cell required to synthesize both LOs and a TTL system clock. The MMIC operates from a 20 MHz external reference and provides overall conversion gain of about 65 dB from a 1575 MHz RF to a 15 MHz second IF. The 1.8 x 1.8 mm MMIC is implemented on a mixed-signal, silicon bipolar cell array and consumes less than 150 mW from a single 3.3V supply.

INTRODUCTION

As the Global Positioning System (GPS) nears completion, the consumer-orientated sales of low-cost receivers is beginning its predicted exponential growth. GPS receiver manufacturers now require inexpensive and highly-integrated components in order to satisfy the mass consumer's demands for low cost, high reliability and small size. In addition, the "handheld" or portable GPS market is largely differentiated by a receiver's battery life and battery type. Unlike previous highly-integrated GPS MMICs [1,2], the MMIC described in this paper addresses not only the issues of cost, size and reliability, but also the specific goal of very low power consumption from a single 3.3V supply. This MMIC is fabricated on a mature silicon bipolar process which is currently used for high-volume, commercial production of discrete MMIC blocks such as amplifiers, mixers, and pre-scalers. The MMIC is packaged in a low-cost, industry-standard 32 lead plastic quad flat package (32PQFP) which occupies less than 1 cm^2 on the GPS receiver board.

The design of the GPS MMIC of this work is based on selecting parameterized-cells on the ROC-01 mixed-signal array. Figure 1 shows the types of cells available on the array. The devices have peak f_T and f_{max} of approximately 14 GHz and 20 GHz respectively. A detailed description of the capabilities of this array is currently being published [3].

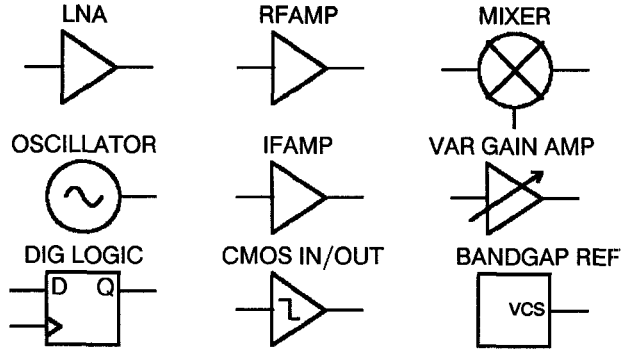

Figure 1. Available Cell Types on ROC-01 Array

The ROC-01 array was developed to implement integrated receive and/or transmit functions primarily for L-band satellite systems such as GPS and for various wireless communication systems operating from 800-2500 MHz. Some specific examples other than GPS could include transceiver MMICs for 900 MHz wireless controls or cellular telephones, 1900 MHz PCN or DECT cordless telephones and 2500 MHz wireless LANs. MMICs implemented on this array can operate from single supply voltages ranging from 3V to 5V depending on the exact specifications. On the ROC-01 array, MMIC blocks such as amplifiers, frequency converters and negative resistance cells (for oscillators) are implemented as pre-determined cells whose attributes (usually determined by resistor values) can be altered in discrete steps similar to speed/power options in commercial digital gate arrays.

IF2

RECEIVER ARCHITECTURE

In this work a generic GPS receiver architecture is shown in Figure 2 with considerable simplifications to highlight the RF/microwave semiconductor components. Note that this architecture is not based on any known proprietary system or signal processing scheme. In fact, to build a working receiver with it requires the development of signal

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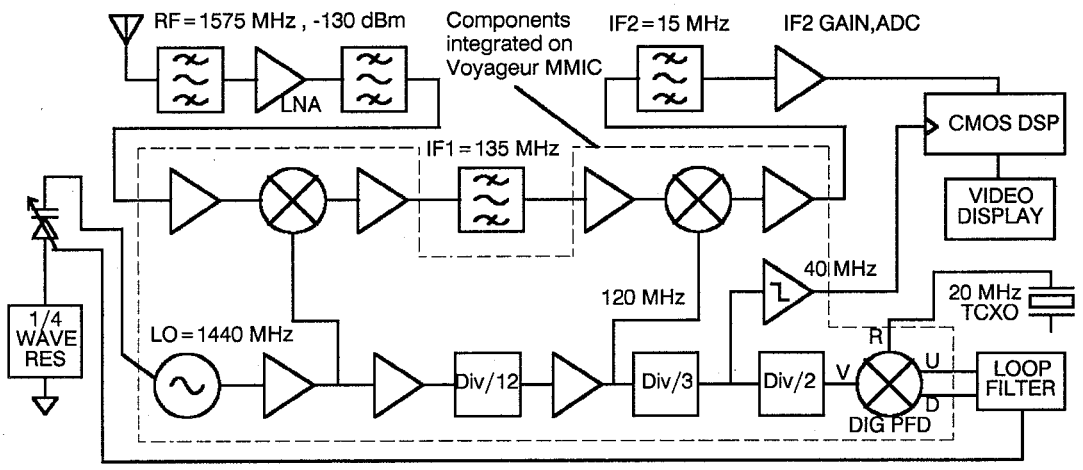

Figure 2. Voyageur Generic GPS Receiver Architecture

processing ICs which are beyond the scope of this work. The discrete blocks within the dashed outline in Figure 2 represent the multitude of functions integrated on the single MMIC of this work (the "Voyageur™" GPS MMIC). These blocks include the mixers and amplifiers for two downconverters, a negative resistance cell, various dividers and buffers, a digital phase-frequency detector and a TTL output. An LNA cell is also available on the ROC-01 array but is not utilized on the Voyageur MMIC due to packaging and power supply limitations. Note that most of the RF function blocks shown in Figure 2 are presently available at low-cost/high-volume as either discretes or single function MMICs. However as Figure 3 illustrates, the integration of these functions on a single MMIC in the 32PQFP package represents a tremendous savings in space and for this specific customer a reduction of over 50 components.

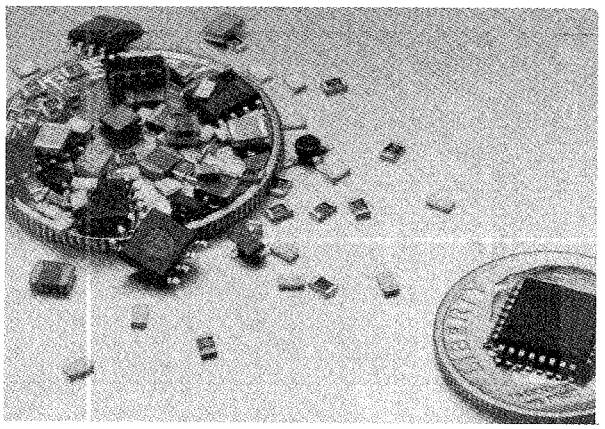

Figure 3. Comparison of Integrated GPS MMIC in 32PQFP (foreground) with Replaced Discretes and Single-Function MMICs for a Specific Customer

The block labeled "CMOS DSP" in Figure 2 usually consists of a standard commercial microprocessor and a custom digital signal processing ASIC. For handheld applications, multiple CMOS vendors are now offering their technologies at the new 3.3V JEDEC standard (future DRAMs will also be at 3.3V). In CMOS circuits the power consumption is reduced by up to 60% at 3.3V compared to 5V operation and better efficiency is obtained with two standard alkaline battery cells (much smaller voltage step-up). In addition the reduction of hot-electron injection effects for short-channel CMOS devices makes the transition to 3.3V virtually inevitable for most high performance CMOS circuits. Thus MMIC suppliers should expect considerable pressure over the next several years from their high-volume commercial customers to produce components that operate from a single 3.3V supply.

Basic specifications for the Voyageur GPS MMIC are summarized in Table 1. The MMIC provides about 65 dB of double-downconversion gain, 12 dB noise figure, synthesis (with external loop filter and tank circuits) of both 1440 MHz and 120 MHz LOs from a 20 MHz reference, and a TTL output drive of a 40 MHz clock. An impedance of 50 Ω is assumed between the downconverters. The second downconverter has an open-collector output which is biased through a 100 μH choke to drive a 500 Ω load. An external resistor of 1000 Ω is used to set the output VSWR. Alternatively, the second downconverter can be externally configured to drive a 50 Ω load from an emitter-follower output with < 2:1 output VSWR and much higher input linearity but with about 12 dB less gain. Note that at VCC=3.3 V and T=25 C the Voyageur MMIC typically consumes less than 45 mA.

First Downconverter $Z_S = Z_L = 50\ \Omega$	
Conversion Gain (RF to IF1)	24 dB
LO/12 Leakage at IF1 Port	-60 dBm
Noise Figure	12 dB
Third-Order Intercept Point	-4 dBm
VSWR of RF (in band) and IF1 Ports	< 2:1
Second Downconverter $Z_S = 50\ \Omega$ $Z_L = 500\ \Omega$	
Conversion Gain (IF1 to IF2)	43 dB
Noise Figure	20 dB
Third-Order Intercept Point	+8 dBm
VSWR of IF1 and IF2 Ports	< 2:1
Freq. Synth. with External Tank and Loop Filter	
SSB Phase Noise of LO at 2 kHz Offset	-70 dBc/Hz
Phase Frequency Detector Output	.2 V/rad
TTL 40 MHz Clock Edges with 10 pF Load	< 8 ns
Supply Current at VCC = 3.3 V	45 mA

Table 1. General Specifications for Voyageur GPS MMIC in the 32PQFP with RF=1575 MHz, LO=1440 MHz.

The exact specifications and frequency plan for the Voyageur GPS MMIC were developed from the compromise of performance versus power dissipation as appropriate for the low-cost commercial market. The spread-spectrum GPS signals at 1575 MHz are nominally received at about -130 dBm (23 dB buried in background noise). Dynamic range of the receiver is usually of little concern due to variations in the GPS signal strength but linearity of the receiver still affects its performance in the presence of non-GPS signals. The linearity of the Voyageur downconverters is believed to be adequate for most consumer-grade applications and was chosen as the maximum available on the ROC-01 array without increasing power consumption significantly over the minimum required for the gain and noise figure goals. Most GPS receivers use about 130 dB of overall gain (plus processing gain in de-spreading) with 20-25 dB gain in the LNA preceding the downconverters. The choice of 12 dB noise figure for the Voyageur MMIC allows the LNA to set the receiver noise figure with little impact from the downconverters. The 65 dB of gain requires the user to provide only another 40-50 dB of inexpensive 15 MHz gain. The actual frequency plan was chosen to derive from a standard low-cost commercial reference of 20 MHz with simple integer order multiples for both LOs to minimize power dissipation and silicon area. The phase noise performance of the synthesized LO is very dependent on the external tank circuit, loop filter and varactor tuning arrangement with the value in Table 1 representing low-cost commercial components. The negative resistance cell is essentially a biased oscillator transistor with an on-chip output. It can be configured externally as either common-base or common-emitter. The low LO/12 leakage from the first downconverter is also important since this output is relatively difficult to filter and if excessive could lead to DC offsets and saturation of the second downconverter. At a minimum, the LO and 2LO output signals of the first downconverter must be filtered since they will saturate the input amplifier of the second downconverter.

3.3V DESIGN CONSIDERATIONS

With a reduced supply voltage, monolithic silicon bipolar circuits are inevitably required to operate at lower values of V_{CE}. Around 3V supply, the exact DC biasing of two-level current-mode circuits such as Gilbert-cell mixers or differential ECL pre-scalers becomes critical to successful operation and optimum performance. Device optimization for low V_{CE} operation is also important and has been utilized on the ROC-01 array.

Space constraints make detailed descriptions of all circuits on the Voyageur MMIC impossible but consider in detail the transistor level schematic of the second downconverter as illustrated in Figure 4. The downconverter consists of a simple differential input amplifier, a Gilbert-cell mixer and an output transistor which can be configured externally as either an amplifier or an emitter-follower output buffer. Not shown in Figure 4 are the bandgap regulator circuit which generates the bias voltage VCS, the digital logic buffer which supplies the second LO (or LO/12) input to the mixer and the input DC biasing circuit for the AC-coupled input amplifier. Note that every resistor shown in Figure 4 is "parameterized" on the array and can be selected from a discrete list of values. The DC levels throughout the downconverter are shown in Figure 4 for the case of VCC=3 V and T=25 C. The basic strategy is to maximize the available V_{CE} on the critical devices by using minimal V_{CE} on the non-critical devices. In the mixer the LO devices are biased with their bases as far from VCC as possible to allow maximum gain from the load resistors. The RF pair of the mixer can operate at very low V_{CE} due to the low impedance of the LO devices as its collector load. The current source devices can be operated virtually into saturation if the bandgap regulator is designed to supply the extra base current for VCS. The DC levels in Figure 4 are intimately related to the I_C-V_{BE} relationship of bipolar devices and the extreme temperature dependence of this relationship can cause disasters at very low supply voltages for wide operating temperature ranges. The downconverter of Figure 4 avoids these problems by optimizing the temperature coefficient of the bandgap regulator voltage VCS to compensate for the temperature

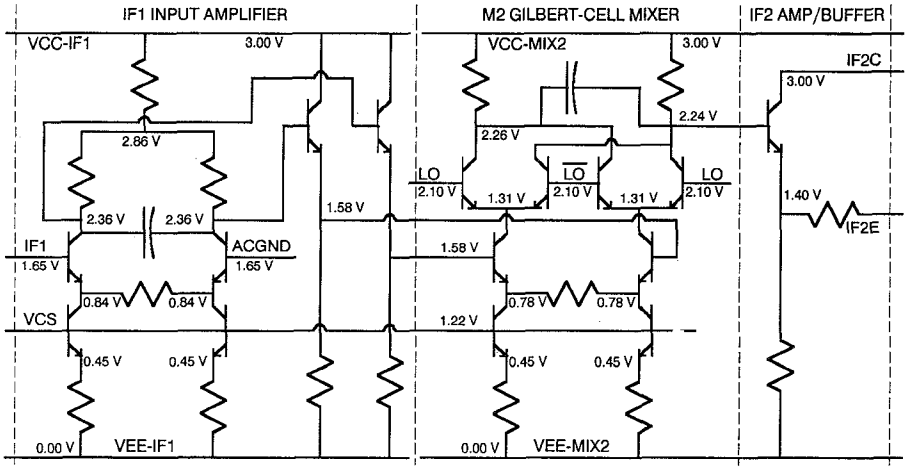

Figure 4. Schematic of Second Downconverter

coefficents of the resistors and the V_{BE} level shifters. Note also from Figure 4 the use of on-chip capacitors which aid stability in the input amplifier and filter out the RF+LO component in the downconverting mixer (effectively doubling the linearity for same current). Physically separate VCC and VEE leads for the downconverter are also required for stability in a low-cost plastic package. The entire second downconverter consumes less than 6 mA at VCC=3 V.

Simulations of gain and input compression point versus VCC and temperature are shown in Figures 5 and 6 for the first and second downconverters respectively. Measured results have agreed well with simulation predictions versus supply voltage but detailed characterizations over temperature are not yet available. The first downconverter is similar to Figure 4 except that the input amplifier is considerably different (a "medium-noise" feedback design) and an emitter-follower output only is used. Overall the design of these downconverters minimizes performance variations due to supply voltage and temperature changes. Note that the reduced gain at low VCC is accomplished with reduced current as well. For example at VCC=2.9 V and T=25 C, the MMIC operates with only about 110 mW of DC power but still provides over 60 dB of conversion gain and all synthesizer functions.

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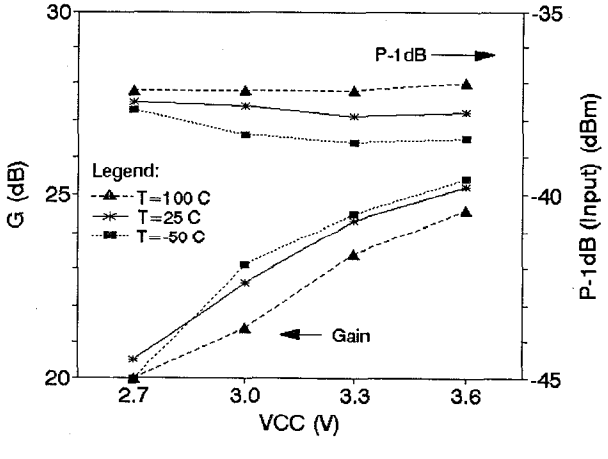

Figure 5. Variation of Gain and Input Compression Point versus VCC and Temperature for First Downconverter

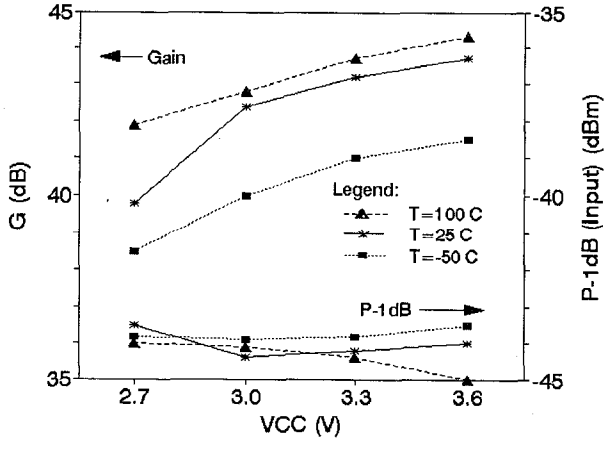

Figure 6. Variation of Gain and Input Compression Point versus VCC and Temperature for Second Downconverter